CLAIMS

1. *(ORIGINAL)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

a signal node to convey an input signal having an input signal value;

amplification circuitry coupled to said signal node, including a variable signal gain responsive to at least one gain control signal having a plurality of values, and responsive to said input signal by providing an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values;

sampling circuitry coupled to said amplification circuitry and responsive to a sampling control signal by sampling said intermediate signal to provide a sample signal having a plurality of values which include at least a maximum and a minimum, and correspond to said plurality of intermediate signal values; and

processing circuitry coupled to said sampling circuitry and responsive to one or more processing control signals by processing said sample signal to provide a processed signal having a value corresponding to said input signal value, wherein said processed signal value represents

said maximum sample signal value when said maximum value fails to traverse a predetermined lower threshold,

said minimum sample signal value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold,

a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold, and

a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

2. *(ORIGINAL)* The apparatus of claim 1, wherein said amplification circuitry comprises:

amplifier circuitry including input and output terminals; and

a variable feedback capacitance coupled between said amplifier circuitry input and output terminals and responsive to one or more of said at least one gain control signal.

3. *(ORIGINAL)* The apparatus of claim 1, wherein said amplification circuitry comprises:

first amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said first amplifier circuitry input and output terminals; and

second amplifier circuitry coupled to said first amplifier circuitry output terminal and having said variable signal gain responsive to said at least one gain control signal.

4. *(ORIGINAL)* The apparatus of claim 1, wherein said amplification circuitry comprises:

amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said amplifier circuitry input and output terminals; and

switched circuitry coupled across said feedback capacitance and including a resistance and a switch responsive to one or more of said at least one gain control signal.

5. *(ORIGINAL)* The apparatus of claim 1, wherein:

said input signal has an input signal charge associated therewith; and

said amplification circuitry comprises

capacitive circuitry, and

a switch coupled between said signal node and said capacitive circuitry, and responsive to one or more of said at least one gain control signal by conveying a predetermined portion of said input signal charge to said capacitive circuitry.

6. *(CURRENTLY AMENDED)* The apparatus of claim 1, wherein said sampling circuitry comprises:

serial switching circuitry coupled to said amplification circuitry and responsive to said sampling control signal by providing a switched signal path for said intermediate signal; and

shunt capacitive circuitry coupled to said ~~amplification~~ serial switching circuitry and responsive to said intermediate signal by charging to provide said sample signal.

7. *(ORIGINAL)* The apparatus of claim 1, wherein said processing circuitry comprises:

analog-to-digital conversion circuitry responsive to one of said one or more processing control signals by converting said sample signal to provide a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

computational circuitry coupled to said analog-to-digital conversion circuitry and responsive to another one or more of said one or more processing control signals and said digital signal by providing said processed signal.

8. *(ORIGINAL)* The apparatus of claim 7, wherein said computational

circuitry comprises:

comparison circuitry responsive to said digital signal by comparing said plurality of digital signal values to said predetermined lower and higher thresholds; and

combining circuitry responsive to said digital signal by selectively combining first and second ones of said plurality of digital signal values to provide a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

9. *(ORIGINAL)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

amplifier means, including variable signal gain, for receiving an input signal having an input signal value and at least one gain control signal having a plurality of values, and in response thereto generating an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values;

sampling means for receiving a sampling control signal and in response thereto sampling said intermediate signal and generating a sample signal having a plurality of values which include at least a maximum and a minimum, and correspond to said plurality of intermediate signal values; and

processor means for receiving one or more processing control signals and in response thereto processing said sample signal and generating a processed signal having a value corresponding to said input signal value, wherein said processed signal value represents

said maximum sample signal value when said maximum value fails to traverse a predetermined lower threshold,

said minimum sample signal value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold, a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold, and

a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

10. *(ORIGINAL)* A method of data signal amplification and processing with multiple signal gains, comprising:

receiving an input signal having an input signal value;

receiving at least one gain control signal having a plurality of values;

generating, in response to said input signal and said at least one gain control signal, an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values;

receiving a sampling control signal and in response thereto sampling said intermediate signal and generating a sample signal having a plurality of values which include at least a maximum and a minimum, and correspond to said plurality of intermediate signal values; and

receiving one or more processing control signals and in response thereto processing said sample signal and generating a processed signal having a value corresponding to said input signal value, wherein said processed signal value represents

said maximum sample signal value when said maximum value fails to traverse a predetermined lower threshold,

said minimum sample signal value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold,

a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold, and

a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

11. *(ORIGINAL)* The method of claim 10, wherein said generating, in response to said input signal and said at least one gain control signal, an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values comprises:

controlling a variable feedback capacitance with said at least one gain control signal; and

generating said intermediate signal as a function of said input signal and said controlled variable feedback capacitance.

12. *(CURRENTLY AMENDED)* The method of claim 10, wherein said generating, in response to said input signal and said at least one gain control signal, an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values comprises:

generating an initial signal in response to said input signal with first amplifier circuitry including a feedback capacitance; and

generating said intermediate signal in response to said initial signal with second amplifier circuitry having ~~said~~ a variable signal gain responsive to said at least one gain control signal.

13. *(ORIGINAL)* The method of claim 10, wherein said generating, in response to said input signal and said at least one gain control signal, an

intermediate signal having a plurality of values corresponding to said plurality of gain control signal values comprises:

selectively discharging a feedback capacitance with said at least one gain control signal; and

generating said intermediate signal as a function of said input signal and said selectively discharged feedback capacitance.

14. *(ORIGINAL)* The method of claim 10, wherein:

said input signal has an input signal charge associated therewith; and

said generating, in response to said input signal and said at least one gain control signal, an intermediate signal having a plurality of values corresponding to said plurality of gain control signal values comprises conveying a predetermined portion of said input signal charge, responsive to one or more of said at least one gain control signal, to capacitive circuitry.

15. *(ORIGINAL)* The method of claim 10, wherein said receiving a sampling control signal and in response thereto sampling said intermediate signal and generating a sample signal having a plurality of values corresponding to said plurality of intermediate signal values comprises:

responding to said sampling control signal by providing a switched signal path for said intermediate signal; and

responding to said intermediate signal by charging shunt capacitive circuitry to provide said sample signal.

16. *(ORIGINAL)* The method of claim 10, wherein said receiving one or more processing control signals and in response thereto processing said sample signal and generating a processed signal having a value corresponding to said input signal value comprises:

responding to one of said one or more processing control signals by converting said sample signal to a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal.

17. *(ORIGINAL)* The method of claim 16, wherein said responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal comprises:

responding to said digital signal by comparing said plurality of digital signal values to said predetermined lower and higher thresholds; and

responding to said digital signal by selectively combining first and second ones of said plurality of digital signal values to generate a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

18. *(ORIGINAL)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

signal acquisition circuitry responsive to an image data signal by providing an acquired data signal;

amplification circuitry coupled to said signal acquisition circuitry and responsive to at least one gain control signal and said acquired data signal by amplifying said acquired data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals;

sampling circuitry coupled to said amplification circuitry and responsive to at least one sampling control signal and said plurality of amplified data signals by sampling said plurality of amplified data signals to produce a corresponding plurality of sampled data signals having a like plurality of values which include at least a maximum and a minimum, and correspond to said plurality of amplified data signals; and

processing circuitry coupled to said sampling circuitry and responsive to one or more criteria signals and one or more of said plurality of sampled data signals by providing a data output signal corresponding to

said maximum sampled data signal value when said maximum value fails to satisfy a first one of a plurality of criteria,

said minimum sampled data signal value when an adjacent larger one of said plurality of sampled data signal values satisfies a second one of said plurality of criteria,

a smaller of mutually adjacent ones of a pair of said plurality of sampled data signal values when a larger one of said pair of sampled data signal values satisfies said second one of said plurality of criteria and said smaller value fails to satisfy said first one of said plurality of criteria, and

a combination of said smaller and larger ones of said pair of sampled data signal values when said larger value satisfies said first one of said plurality of criteria and fails to satisfy said second one of said plurality of criteria.

19. *(ORIGINAL)* The apparatus of claim 18, wherein said amplification circuitry comprises:

amplifier circuitry including input and output terminals; and

a variable feedback capacitance coupled between said amplifier circuitry input and output terminals and responsive to one or more of said at least one gain control signal.

20. *(CURRENTLY AMENDED)* The apparatus of claim 18, wherein said amplification circuitry comprises:

first amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said first amplifier circuitry input and output terminals; and

second amplifier circuitry coupled to said first amplifier circuitry output terminal and having ~~said~~ a variable signal gain responsive to said at least one gain control signal.

21. *(ORIGINAL)* The apparatus of claim 18, wherein said amplification circuitry comprises:

amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said amplifier circuitry input and output terminals; and

switched circuitry coupled across said feedback capacitance and including a resistance and a switch responsive to one or more of said at least one gain control signal.

22. *(ORIGINAL)* The apparatus of claim 18, wherein:

said input signal has an input signal charge associated therewith; and

said amplification circuitry comprises

capacitive circuitry, and

a switch coupled between said signal node and said capacitive circuitry, and responsive to one or more of said at least one gain control signal by conveying a predetermined portion of said input signal charge to said capacitive circuitry.

23. *(CURRENTLY AMENDED)* The apparatus of claim 18, wherein said sampling circuitry comprises:

serial switching circuitry coupled to said amplification circuitry and responsive to said sampling control signal by providing a switched signal path for said intermediate signal; and

shunt capacitive circuitry coupled to said ~~amplification~~ serial switching circuitry and responsive to said intermediate signal by charging to provide said sample signal.

24. *(ORIGINAL)* The apparatus of claim 18, wherein said processing circuitry comprises:

analog-to-digital conversion circuitry responsive to one of said one or more processing control signals by converting said sample signal to provide a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

computational circuitry coupled to said analog-to-digital conversion circuitry and responsive to another one or more of said one or more processing control signals and said digital signal by providing said processed signal.

25. *(ORIGINAL)* The apparatus of claim 24, wherein said computational circuitry comprises:

comparison circuitry responsive to said digital signal by comparing said plurality of digital signal values to said predetermined lower and higher thresholds; and

combining circuitry responsive to said digital signal by selectively combining first and second ones of said plurality of digital signal values to provide a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

26. *(ORIGINAL)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

signal acquisition means for acquiring a data signal;

amplifier means for amplifying said acquired data signal with a plurality of signal gains and generating a corresponding plurality of amplified data signals;

sampling means for sampling said plurality of amplified data signals and generating a corresponding plurality of sampled data signals having a like plurality of values which include at least a maximum and a minimum, and correspond to said plurality of amplified data signals; and

processor means for processing one or more of said plurality of sampled data signals and generating a data output signal corresponding to

said maximum sampled data signal value when said maximum value fails to satisfy a first one of a plurality of criteria,

said minimum sampled data signal value when an adjacent larger one of said plurality of sampled data signal values satisfies a second one of said plurality of criteria,

a smaller of mutually adjacent ones of a pair of said plurality of sampled data signal values when a larger one of said pair of sampled data signal values satisfies said second one of said plurality of criteria and said smaller value fails to satisfy said first one of said plurality of criteria, and

a combination of said smaller and larger ones of said pair of sampled data signal values when said larger value satisfies said first one of said plurality of criteria and fails to satisfy said second one of said plurality of criteria.

27. *(ORIGINAL)* A method of data signal amplification and processing with multiple signal gains, comprising:

acquiring an image data signal;

amplifying said image data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals;

sampling said plurality of amplified data signals to produce a corresponding plurality of sampled data signals having a like plurality of values which include at least a maximum and a minimum, and correspond to said plurality of amplified data signals;

comparing one or more of said plurality of sampled data signal values to one or more of a plurality of criteria; and

providing a data output signal corresponding to

said maximum sampled data signal value when said maximum value fails to satisfy a first one of said plurality of criteria,

said minimum sampled data signal value when an adjacent larger one of said plurality of sampled data signal values satisfies a second one of said plurality of criteria,

a smaller of mutually adjacent ones of a pair of said plurality of sampled data signal values when a larger one of said pair of sampled data signal values satisfies said second one of said plurality of criteria and said smaller value fails to satisfy said first one of said plurality of criteria, and

a combination of said smaller and larger ones of said pair of sampled data signal values when said larger value satisfies said first one of said plurality of criteria and fails to satisfy said second one of said plurality of criteria.

28. *(ORIGINAL)* The method of claim 27, wherein said amplifying said image data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals comprises:

controlling a variable feedback capacitance; and

generating said plurality of amplified data signals as a function of said image data signal and said controlled variable feedback capacitance.

29. *(ORIGINAL)* The method of claim 27, wherein said amplifying said image data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals comprises:

generating an initial signal in response to said image data signal with first amplifier circuitry including a feedback capacitance; and

generating said plurality of amplified data signals in response to said initial signal with second amplifier circuitry having said plurality of signal gains.

30. *(ORIGINAL)* The method of claim 27, wherein said amplifying said image data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals comprises:

selectively discharging a feedback capacitance; and

generating said plurality of amplified data signals as a function of said image data signal and said selectively discharged feedback capacitance.

31. *(ORIGINAL)* The method of claim 27, wherein:

said image data signal has a signal charge associated therewith; and

said amplifying said image data signal with a plurality of signal gains to produce a corresponding plurality of amplified data signals comprises conveying a plurality of predetermined portions of said image data signal charge to capacitive circuitry.

32. *(ORIGINAL)* The method of claim 27, wherein said sampling said plurality of amplified data signals to produce a corresponding plurality of sampled data signals having a like plurality of values which include at least a maximum and a minimum, and correspond to said plurality of amplified data signals comprises:

switching said plurality of amplified data signals; and

charging shunt capacitive circuitry with said switched plurality of amplified data signals to generate said plurality of sampled data signals.

33. *(ORIGINAL)* The method of claim 27, wherein said comparing one

or more of said plurality of sampled data signal values to one or more of a plurality of criteria comprises comparing one or more of said plurality of sampled data signal values to one or more of a plurality of reference signals corresponding to predetermined lower and higher thresholds.

34. *(ORIGINAL)* The method of claim 27, wherein said providing a data output signal corresponding to a combination of said smaller and larger ones of said pair of sampled data signal values when said larger value satisfies said first one of said plurality of criteria and fails to satisfy said second one of said plurality of criteria comprises selectively combining a portion of said plurality of sampled data signal values.

35. *(NEW)* An apparatus including data signal amplifier circuitry with multiple signal gains, comprising:

sampling amplifier circuitry responsive to at least one control signal and an input signal having an input signal value by providing at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value; and

processing circuitry coupled to said sampling amplifier circuitry and responsive to said at least one sample signal and one or more processing control signals by processing said at least one sample signal to provide a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

said maximum sample signal value,
said minimum sample signal value,
a first one of said plurality of sample signal values, and
a combination of said first one and a second one of said plurality of

sample signal values.

36. *(NEW)* The apparatus of claim 35, wherein said processed signal value represents:

said maximum sample signal value when said maximum value fails to traverse a predetermined lower threshold;

said minimum sample signal value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold;

a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold; and

a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

37. *(NEW)* The apparatus of claim 35, wherein said sampling amplifier circuitry comprises:

amplifier circuitry including input and output terminals; and

a variable feedback capacitance coupled between said amplifier circuitry input and output terminals and responsive to one or more of said at least one control signal.

38. *(NEW)* The apparatus of claim 35, wherein said sampling amplifier circuitry comprises:

first amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said first amplifier circuitry input and output terminals; and second amplifier circuitry coupled to said first amplifier circuitry output terminal and having said variable signal gain responsive to at least one of said at least one control signal.

39. *(NEW)* The apparatus of claim 35, wherein said sampling amplifier circuitry comprises:

amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said amplifier circuitry input and output terminals; and

switched circuitry coupled across said feedback capacitance and including a resistance and a switch responsive to one or more of said at least one control signal.

40. *(NEW)* The apparatus of claim 35, wherein:

said input signal has an input signal charge associated therewith; and

said sampling amplifier circuitry comprises

a signal node to convey said input signal,

capacitive circuitry, and

a switch coupled between said signal node and said capacitive circuitry, and responsive to one or more of said at least one control signal by conveying a predetermined portion of said input signal charge to said capacitive circuitry.

41. *(NEW)* The apparatus of claim 35, wherein said sampling amplifier circuitry comprises:

serial switching circuitry responsive to one of said at least one control signal by providing a switched signal; and

shunt capacitive circuitry coupled to said serial switching circuitry and responsive to said switched signal by charging to provide said at least one sample signal.

42. *(NEW)* The apparatus of claim 35, wherein said processing circuitry comprises:

analog-to-digital conversion circuitry responsive to one of said one or more processing control signals by converting said sample signal to provide a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

computational circuitry coupled to said analog-to-digital conversion circuitry and responsive to another one or more of said one or more processing control signals and said digital signal by providing said processed signal.

43. *(NEW)* The apparatus of claim 42, wherein said computational circuitry comprises:

comparison circuitry responsive to said digital signal by comparing said plurality of digital signal values to predetermined lower and higher thresholds; and

combining circuitry responsive to said digital signal by selectively combining first and second ones of said plurality of digital signal values to provide a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

44. *(NEW)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

sampling amplifier means for receiving at least one control signal and an input signal having an input signal value and in response thereto providing at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value;

and

processor means for receiving said at least one sample signal and one or more processing control signals and in response thereto processing said at least one sample signal and providing a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

said maximum sample signal value,

said minimum sample signal value,

a first one of said plurality of sample signal values, and

a combination of said first one and a second one of said plurality of sample signal values.

45. *(NEW)* A method of data signal amplification and processing with multiple signal gains, comprising:

receiving at least one control signal;

receiving an input signal having an input signal value;

generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value; and

receiving one or more processing control signals and in response thereto processing said at least one sample signal and generating a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

said maximum sample signal value,

said minimum sample signal value,

a first one of said plurality of sample signal values, and

a combination of said first one and a second one of said plurality of sample signal values.

46. *(NEW)* The method of claim 45, wherein said processed signal value represents:

said maximum sample signal value when said maximum value fails to traverse a predetermined lower threshold;

said minimum sample signal value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold;

a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold; and

a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

47. *(NEW)* The method of claim 45, wherein said generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value comprises:

controlling a variable feedback capacitance with one or more of said at least one control signal; and

generating said at least one sample signal as a function of said input signal and said controlled variable feedback capacitance.

48. *(NEW)* The method of claim 45, wherein said generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value comprises:

generating an initial signal in response to said input signal with first amplifier circuitry including a feedback capacitance; and

generating said at least one sample signal in response to said initial signal with second amplifier circuitry having a variable signal gain responsive to at least one of said plurality control signals.

49. *(NEW)* The method of claim 45, wherein said generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value comprises:

selectively discharging a feedback capacitance with at least one of said at least one control signal; and

generating said at least one sample signal as a function of said input signal and said selectively discharged feedback capacitance.

50. *(NEW)* The method of claim 45, wherein:

said input signal has an input signal charge associated therewith; and

said generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value comprises conveying a predetermined portion of said input signal charge, responsive to one or more of said at least one control signal, to capacitive circuitry.

51. *(NEW)* The method of claim 45, wherein said generating, in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values, including maximum and minimum sample signal values, and corresponding to said input signal value comprises:

responding to one of said at least one control signal by providing a switched signal; and

responding to said switched signal by charging shunt capacitive circuitry to provide said at least one sample signal.

52. *(NEW)* The method of claim 45, wherein said receiving one or more processing control signals and in response thereto processing said at least one sample signal and generating a processed signal having a value corresponding to said input signal value comprises:

responding to one of said one or more processing control signals by converting said at least one sample signal to a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal.

53. *(NEW)* The method of claim 52, wherein said responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal comprises:

responding to said digital signal by comparing said plurality of digital signal values to predetermined lower and higher thresholds; and

responding to said digital signal by selectively combining first and second ones of said plurality of digital signal values to generate a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

54. *(NEW)* An apparatus including data signal amplifier circuitry with multiple signal gains, comprising:

sampling amplifier circuitry with a plurality of signal gains, including at least maximum and minimum signal gains, and responsive to at least one control signal and an input signal having an input signal value by providing at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value; and

processing circuitry coupled to said sampling amplifier circuitry and responsive to said at least one sample signal and one or more processing control signals by processing said at least one sample signal to provide a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

a first value corresponding to said minimum signal gain,

a second value corresponding to said maximum signal gain,

a third value corresponding to a first one of said plurality of signal gains, and

a fourth value corresponding to a combination of said first one and a second one of said plurality of signal gains.

55. *(NEW)* The apparatus of claim 54, wherein:

said plurality of sample signal values includes maximum and minimum sample signal values; and

said processed signal value represents

said first value when said maximum sample signal value fails to traverse a predetermined lower threshold,

said second value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold,

said third value as a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold, and

said fourth value as a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

56. *(NEW)* The apparatus of claim 54, wherein said sampling amplifier circuitry comprises:

amplifier circuitry including input and output terminals; and

a variable feedback capacitance coupled between said amplifier circuitry input and output terminals and responsive to one or more of said at least one control signal.

57. *(NEW)* The apparatus of claim 54, wherein said sampling amplifier circuitry comprises:

first amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said first amplifier circuitry input and output terminals; and

second amplifier circuitry coupled to said first amplifier circuitry output terminal and having said variable signal gain responsive to at least one of said at least one control signal.

58. *(NEW)* The apparatus of claim 54, wherein said sampling amplifier circuitry comprises:

amplifier circuitry including input and output terminals;

a feedback capacitance coupled between said amplifier circuitry input and output terminals; and

switched circuitry coupled across said feedback capacitance and including a resistance and a switch responsive to one or more of said at least one control signal.

59. *(NEW)* The apparatus of claim 54, wherein:

said input signal has an input signal charge associated therewith; and

said sampling amplifier circuitry comprises

a signal node to convey said input signal,

capacitive circuitry, and

a switch coupled between said signal node and said capacitive circuitry, and responsive to one or more of said at least one control signal by conveying a predetermined portion of said input signal charge to said capacitive circuitry.

60. *(NEW)* The apparatus of claim 54, wherein said sampling amplifier circuitry comprises:

serial switching circuitry responsive to one of said at least one control signal by providing a switched signal; and

shunt capacitive circuitry coupled to said serial switching circuitry and responsive to said switched signal by charging to provide said at least one sample signal.

61. *(NEW)* The apparatus of claim 54, wherein said processing circuitry comprises:

analog-to-digital conversion circuitry responsive to one of said one or more processing control signals by converting said sample signal to provide a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

computational circuitry coupled to said analog-to-digital conversion circuitry and responsive to another one or more of said one or more processing control signals and said digital signal by providing said processed signal.

62. *(NEW)* The apparatus of claim 61, wherein said computational circuitry comprises:

comparison circuitry responsive to said digital signal by comparing said plurality of digital signal values to predetermined lower and higher thresholds; and

combining circuitry responsive to said digital signal by selectively combining first and second ones of said plurality of digital signal values to provide a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

63. *(NEW)* An apparatus including data signal amplification and processing circuitry with multiple signal gains, comprising:

sampling amplifier means with a plurality of signal gains, including at least maximum and minimum signal gains, for receiving at least one control signal and an input signal having an input signal value and in response thereto providing at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value; and

processor means for receiving said at least one sample signal and one or more processing control signals and in response thereto processing said at least one sample signal and providing a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

a first value corresponding to said minimum signal gain,

a second value corresponding to said maximum signal gain,

a third value corresponding to a first one of said plurality of signal gains, and

a fourth value corresponding to a combination of said first one and a second one of said plurality of signal gains.

64. *(NEW)* A method of data signal amplification and processing with multiple signal gains, comprising:

receiving at least one control signal;

receiving an input signal having an input signal value;

generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value; and

receiving one or more processing control signals and in response thereto processing said at least one sample signal and generating a processed signal having a value corresponding to said input signal value;

wherein said processed signal value represents one of a plurality of values which includes

a first value corresponding to said minimum signal gain,

a second value corresponding to said maximum signal gain,

a third value corresponding to a first one of said plurality of signal gains, and

a fourth value corresponding to a combination of said first one and a second one of said plurality of signal gains.

65. *(NEW)* The method of claim 64, wherein:

said plurality of sample signal values includes maximum and minimum sample signal values; and

said processed signal value represents

said first value when said maximum sample signal value fails to traverse a predetermined lower threshold,

said second value when an adjacent larger one of said plurality of sample signal values traverses a predetermined higher threshold,

said third value as a smaller of mutually adjacent ones of a pair of said plurality of sample signal values when a larger one of said pair of sample signal values traverses said predetermined higher threshold and said smaller value fails to traverse said predetermined lower threshold, and

said fourth value as a combination of said smaller and larger ones of said pair of sample signal values when said larger value traverses said predetermined lower threshold and fails to traverse said predetermined higher threshold.

66. *(NEW)* The method of claim 64, wherein said generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value comprises:

controlling a variable feedback capacitance with one or more of said at least one control signal; and

generating said at least one sample signal as a function of said input signal and said controlled variable feedback capacitance.

67. *(NEW)* The method of claim 64, wherein said generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value comprises:

generating an initial signal in response to said input signal with first amplifier circuitry including a feedback capacitance; and

generating said at least one sample signal in response to said initial signal with second amplifier circuitry having a variable signal gain responsive to at least one of said plurality control signals.

68. *(NEW)* The method of claim 64, wherein said generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value comprises:

selectively discharging a feedback capacitance with at least one of said at least one control signal; and

generating said at least one sample signal as a function of said input signal and said selectively discharged feedback capacitance.

69. *(NEW)* The method of claim 64, wherein:

said input signal has an input signal charge associated therewith; and

said generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value comprises conveying a predetermined portion of said input signal charge, responsive to one or more of said at least one control signal, to capacitive circuitry.

70. *(NEW)* The method of claim 64, wherein said generating, in conformance with a plurality of signal gains, including at least maximum and minimum signal gains, and in response to said at least one control signal and said input signal, at least one sample signal having a plurality of sample signal values related to said plurality of signal gains and corresponding to said input signal value comprises:

responding to one of said at least one control signal by providing a switched signal; and

responding to said switched signal by charging shunt capacitive circuitry to provide said at least one sample signal.

71. *(NEW)* The method of claim 64, wherein said receiving one or more processing control signals and in response thereto processing said at least one sample signal and generating a processed signal having a value corresponding to said input signal value comprises:

responding to one of said one or more processing control signals by converting said at least one sample signal to a digital signal having a plurality of values corresponding to said plurality of sample signal values; and

responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal.

72. *(NEW)* The method of claim 71, wherein said responding to another one or more of said one or more processing control signals and said digital signal by generating said processed signal comprises:

responding to said digital signal by comparing said plurality of digital signal values to predetermined lower and higher thresholds; and responding to said digital signal by selectively combining first and second ones of said plurality of digital signal values to generate a combination signal corresponding to said combination of said first and second ones of said plurality of sample signal values.

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